C²I² Systems

CCII Systems (Pty) Ltd Registration No. 1990/005058/07

Communications
Computer Intelligence
Integration

Hardware Reference Manual

for the

High-Speed Serial I/O PMC Adapter

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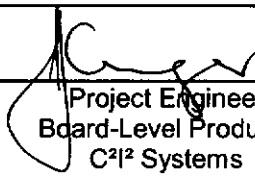
Completed by X. Kruger	 Project Engineer Board-Level Products C²I² Systems	2010-03-04
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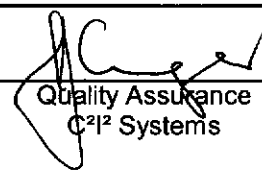
Accepted by X. Kruger	 Quality Assurance C²I² Systems	2010-03-04

Amendment History

Issue	Description	Date	ECP No.
0.1	First release.	2000-07-14	-
1.0	General update to document.	2002-02-13	-
1.1	Added Ordering and Part Number Information for the mating Molex Frontpanel Connector.	2003-10-31	CCII/HSS/6-ENG/012
1.2	Hyphenated the word High-Speed in title.	2009-05-27	CCII/BLPGEN/6-ECP/015
1.3	Improve document naming consistency	2009-12-21	CCII/HSS/6-ECP/019

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Abbreviations and Acronyms

BDM	Background Debug and Monitoring
BRG	Baud Rate Generator
CC	Conduction-Cooled
CCII	Communications Computer Intelligence Integration
COM	Commercial
CRC	Cyclic Redundancy Check
EEPROM	Electrically Erasable Programmable Read Only Memory
FP	Frontpanel
HDLC	High-Level Data Link Control
HSS	High-Speed Serial
I/O	Input / Output
IND	Industrial
PCI	Peripheral Component Interconnect
PMC	PCI Mezzanine Card
RAM	Random Access Memory
SCC	Serial Communication Controller
SDLC	Synchronous Data Link Control
SIG	Special Interest Group
SMC	Serial Management Controller
UART	Universal Asynchronous Receiver/Transmitter

1. Identification

This document is the technical reference manual for the C²I² Systems' High-Speed Serial (HSS) PCI Mezzanine Card (PMC) Input / Output (I/O) Adapter.

1.1 System Overview

The HSS PMC I/O Adapter provides four simultaneous, high-speed, bi-directional serial communication channels. The adapter is available in both forced-air and conduction-cooled versions.

1.2 Document Overview

This document gives an overview of the HSS PMC I/O Adapter functional building blocks in, as well as a brief description of each block. The external interfaces of the HSS PMC I/O Adapter are specified in Paragraph 4. Paragraph 5 concludes by describing the hardware as seen by the embedded or host programmer.

2. Applicable and Reference Documents

2.1 Applicable Documents

2.1.1 IEEE Std 1386-2001, *IEEE Standard for a Common Mezzanine Card (CMC) Family*, dated 2001-06-14.

2.1.2 PCI Special Interest Group, *PCI Local Bus Specification*, Rev. 2.2, dated 1998-12-18.

2.2 Reference Documents

2.2.1 QSpan™ (CA91C860B, CA91L860B) PCI to Motorola Processor Bridge Manual.

2.2.2 MPC860 PowerQUICC(tm) User's Manual, Rev 1, 07/98.

2.2.3 C²I² Systems document CCII/HSS/6-MAN/002, titled User Manual for the High-Speed Serial I/O Adapter VxWorks Software Driver.

3. Functional Description

3.1 Specification

Designation	Description	
CCII/SIO/PMC/4P/FP/COM CCII/SIO/PMC/4P/FP/IND	0 C to +55 C : Commercial Temp Spec. *-40 C to +85 C : Extended Temp Spec.*	PMC Intelligent High-Speed Serial Front I/O (4-Channel) *Conventionally-Cooled*
CCII/SIO/PMC/4P/BP/COM CCII/SIO/PMC/4P/BP/CC	0 C to +55 C : Commercial Temp Spec. *-40 C to +85 C : Extended Temp Spec.*	PMC Intelligent High-Speed Serial Rear I/O (4-Channel) *Conduction-Cooled*
Logic Interface	PCI Mezzanine Card (PMC) Interface 32-bit PCI Interface compliant with PCI Revision 2.1	
Size	Single-size CMC, 75 mm wide, 50 mm deep (i.a.w. IEEE P1386.1)	
Number of Serial Channels	4 x SCCs (Serial Communication Controllers) for high-speed serial links *2 x SMCs (Serial Management Controllers) for lower-speed serial links (UART)*	
Temperature Range **Operating** Non-Operating	0 C to +55 C : Commercial version *-40 C to +85 C : Extended temperature version* *-55 C to +125 C*	
Vibration CCII/SIO/PMC/4P/BP/CC	Sine : 5 g (peak) 15 to 2 kHz - 10 minutes per axis Random : 0,02 g^2/Hz at 15 to 2 kHz - 60 minutes per axis	
Shock CCII/SIO/PMC/4P/BP/CC	20 g for 11 ms (half sine shock pulses)	
MTBF CCII/SIO/PMC/4P/BP/CC	Figures according to MIL-HDBK-217F, Parts Count Method : Ground Mobile T_j = 65 C, T_a = 45 C 32 000 hours Naval, Sheltered T_j = 60 C, T_a = 40 C 47 000 hours Airborne, Inhabited Cargo T_j = 75 C, T_a = 55 C 31 000 hours	
Interrupts	PCI INT A	
Power Requirements	800 mA at 5 V DC +/- 5 %	

Table I : HSS Specifications

3.2 Functional Block Diagram

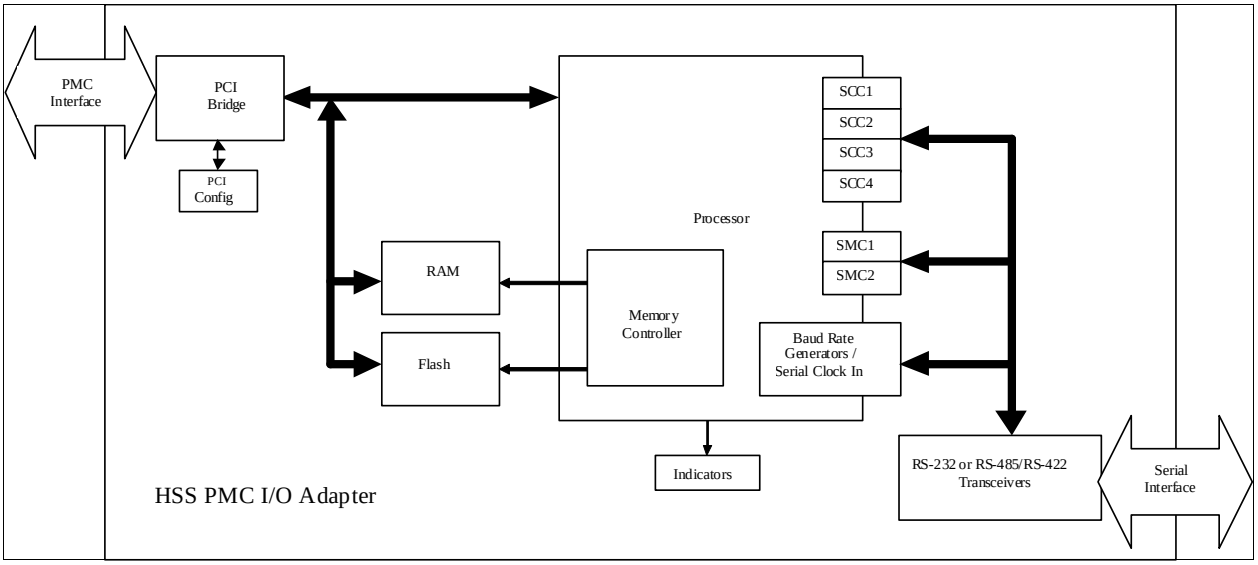

Figure 1 : HSS PMC I/O Adapter Block Diagram

- The HSS PMC I/O Adapter consists of the following functional elements :
- PMC Interface
- PCI Bridge
- PCI Configuration EEPROM
- Processor
- RAM
- Flash
- Indicators
- Four Serial Communication Controllers (SCC)
- Two Serial Management Controllers (SMC)
- Four Baud Rate Generators (BRG) and four external serial clock inputs
- RS-232 and/or RS-422/485 Transceivers
- Serial Interface

3.3 PMC Interface

The PMC interface allows the HSS PMC I/O Adapter to be fitted on any host carrier card conforming to the PMC specification. The serial interfaces of the HSS PMC I/O Adapter are routed through the PMC connector Pn4 [Figure 2].

The interface consists of a PCI bus interface and a number of bus-mode signals. On the HSS PMC I/O Adapter the bus-mode signalling is implemented using a PAL device. The bus-mode signalling prevents the adapter from operating on a non-PCI bus and allows the host to sense the presence of an adapter in a PMC slot.

Refer to the PMC specification [2.1.1] for a complete description of the PCI interface signals and to the CMC specification [2.1.2] for information on bus-mode signalling.

3.4 PCI Bridge

The PCI bridge translates memory access requests on the PCI bus to requests on the local bus and vice versa. The HSS PMC I/O Adapter uses the QSpan™ chip from Tundra Semiconductor Corporation to bridge the PowerQUICC™ processor from Motorola to the PCI bus.

Refer to the Qspan™ reference manual [2.2.2] for more information.

3.5 PCI Configuration

PCI configuration information is stored in the PCI Configuration EEPROM. The information in the EEPROM is loaded by the PCI bridge when the adapter is reset (either at power-up or during use). The EEPROM must be programmed with valid values before the HSS PMC I/O Adapter will be plug-and-play compatible.

To program the PCI configuration EEPROM refer to [2.2.1, page 2-69].

The HSS PMC I/O Adapter uses the following default configuration space values :

Offset	Default Value	Description
0x00	0x10E3	PCI SIG allocated vendor identifier.
0x02	0x0860 or 0x0862	Device Identifier
0x10	--	Base address of HSS PMC I/O Adapter assigned by host adapter.

Table II : PCI Configuration

3.6 Processor

The HSS PMC I/O Adapter uses the PowerQUICC™ processor from Motorola to provide four high-speed and two lower-speed serial ports with protocol processing. The PowerQUICC™ has a built-in memory controller for glue-less connection to static RAM and flash memory. For serial clock generation, four built-in baud rate generators are provided and provision is made for four external serial clock inputs.

Refer to the PowerQUICC™ reference manual [2.2.2] for more information.

3.7 PMC Interface

The HSS PMC I/O Adapter interfaces to the host via a 32-bit PCI PMC interface. For a complete list of signals and connector pin-outs refer to the PMC Specification [2.1.1].

3.8 Random Access Memory (RAM)

The HSS PMC I/O Adapter provides 1 MByte of static RAM. This memory is used at run-time for processing interrupts and for passing control information to and from the host adapter.

3.9 Flash Memory

The HSS PMC I/O Adapter provides 2 MBytes of programmable flash memory. The flash memory is used as boot device and holds the adapter firmware. The firmware is initially programmed using the BDM port of the PowerQUICC™ but can be upgraded from the host adapter over the PCI bus.

3.10 Indicators

The HSS PMC I/O Adapter provides five indicators for reporting hardware and software status. Refer to [Figure 2] for indicator placement. The following table describes the use of each indicator :

Indicator	Description
D2	Reset indicator
D3	User indicator 1
D4	User indicator 2
D5	3,3 V Power indicator
D6	5 V Power indicator

Table III : HSS PMC I/O Adapter Indicators

3.11 Serial Communication Controller (SCC)

The HSS PMC I/O Adapter provides four high-speed SCC channels enabling it to support a large number of serial protocols. The following serial protocols are supported:

- Ethernet/IEEE 802.3 supporting full 10-Mbit/s operation (One SCC only)
- HDLC/SDLC
- HDLC bus (implements an HDLC-based local area network (LAN))
- Asynchronous HDLC to support PPP (point-to-point protocol)
- AppleTalk
- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Serial infrared (IrDA)
- Binary synchronous communication (BISYNC)
- Totally transparent (bit streams)
- Totally transparent (frame based with optional cyclic redundancy check (CRC))

3.12 Serial Management Controller (SMC)

The HSS PMC I/O Adapter provides two SMC channels for lower-speed serial communication requiring little protocol processing. The SMC channels can be used in UART or transparent mode.

3.13 Serial Clocks

The HSS PMC I/O Adapter has four independent Baud Rate Generators (BRGs) that may be set to any valid baud rate. Sample baud rates are given in the following table :

1 200, 4 800, 9 600, 19 200, 38 400, 76 800	UART (RS-232)
All the above and 153 600, 307 200, 614 400, 1 228 800	UART (RS-485/RS-422)
All the above and 2 456 700, 4 915 200, 9 830 400	HDLC

Table IV : Baud Rates

The baud rate generators can be set to any value between 1 200 bit/s and 20 Mbit/s, but will only be exact for the values given above since clock division is used to generate the serial clock rates.

The HSS PMC I/O Adapter also takes four serial clock inputs, allowing the user to supply custom clock rates to any of the SCC or SMC. Clock division does not limit these input clocks, but their maximum values are dependent on the electrical interface as well as the protocols chosen. Refer to [2.2.2, Appendix B] for protocol limitations.

3.14 Serial Interface

The HSS PMC I/O Adapter communicates with the user through rear I/O, using the Pn4 connector on the PMC [See Figure 2], or through a 120-pin Molex connector on HSS Frontpanel (FP) adapters [See Figure 3]. The pin-outs and signal descriptions are given in [4.2].

3.15 Build Options

The HSS Back Panel I/O PMC may be ordered with either a RS-232 electrical interface or a RS-422/485 electrical interface. The HSS Frontpanel PMC I/O supports both electrical interfaces for each channel, with the user selecting the correct electrical interface in software. Refer to [2.2.3] for more information.

Cables for RS-422/485 need to be terminated as required since the HSS PMC I/O Adapter does not have any terminating resistors.

HSS Part No.	SCC	SMC
CCII/SIO/PMC/4P/BP/XX/44	RS-485	RS-485
CCII/SIO/PMC/4P/BP/XX/42	RS-485	RS-232
CCII/SIO/PMC/4P/BP/XX/22	RS-232	RS-232
CCII/SIO/PMC/4P/BP1/XX	RS-485	RS-232
CCII/SIO/PMC/4P/FP/XX	AUTO [See 2.2.3]	AUTO [See 2.2.3]

Table V : Build Options

Note : XX = CC or COM.

4. **Connector Pin Assignments**

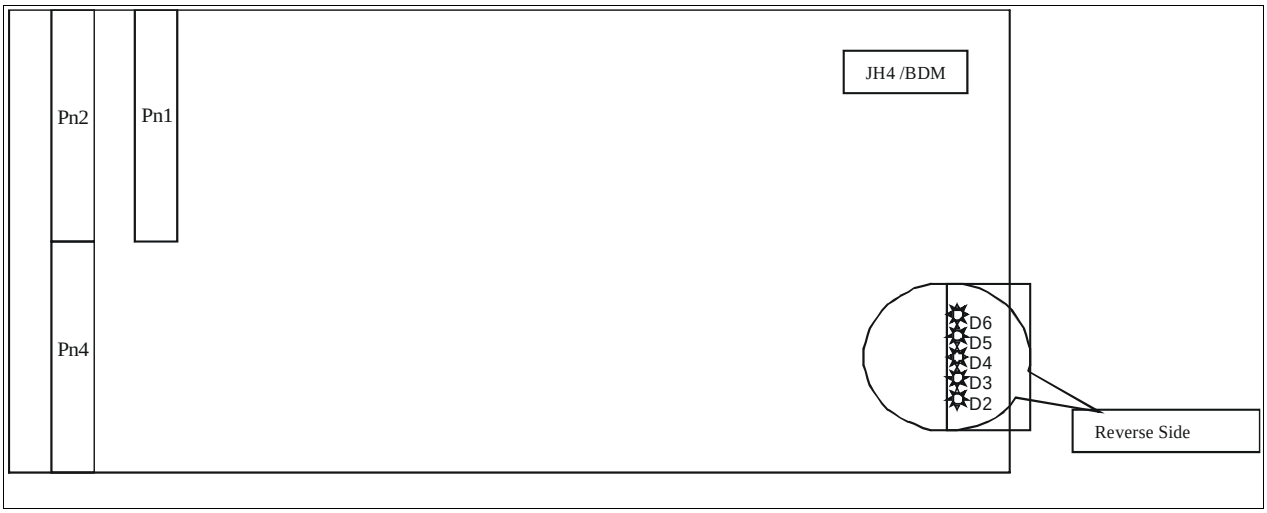

Figure 2 : Connector Pin and Indicator Positions

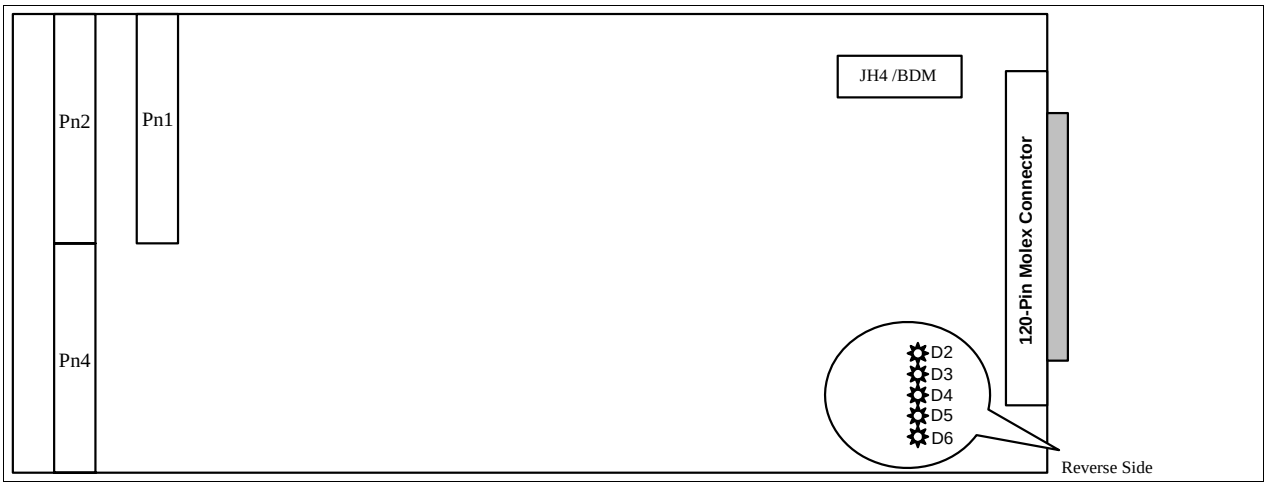

Figure 3 : HSS Frontpanel Pin and Indicator Positions

4.1 PMC Connectors

Pin No.	Signal Name	Signal Name	Pin No.
1	TCK	-12 V	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5 V	8
9	INTD#	PCI-RSVD	10
11	Ground	PCI-RSVD	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5 V	18
19	V I/O	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5 V	30
31	VI/O	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5 V	38
39	Ground	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	Ground	44
45	VI/O	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5 V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	VI/O	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5 V	62
63	Ground	REQ64#	64

Table VI : Pn1 - 32-bit PCI

Pin No.	Signal Name	Signal Name	Pin No.
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD	8
9	PCI-RSVD	PCI-RSVD	10
11	BUSMODE2#	+3,3 V	12
13	RST#	BUSMODE3#	14
15	+3,3 V	BUSMODE4#	16
17	PCI-RSVD	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3,3 V	24
25	IDSEL	AD[23]	26
27	+3,3 V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34
35	TRDY#	+3,3 V	36
37	Ground	STOP#	38
39	PERR#	Ground	40
41	+3,3 V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3,3 V	50
51	AD[07]	PMC-RSVD	52
53	+3,3 V	PMC-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PMC-RSVD	58
59	Ground	PMC-RSVD	60
61	ACK64#	+3,3 V	62
63	Ground	PMC-RSVD	64

Table VII : Pn2 - 32-bit PCI

4.2 Serial I/O Connector

Netlist Name	RS-232 Name	RS-422/485 Name	PMC I/F Pn4 Pin No.	HCC PMC Site No. 1 P0 Pin No. (DY4 178/179)	HCC PMC Site No. 2 P2 Pin No.	Frontpanel Connections Molex Pin No. (HSS FP Adapters)
PortA1	CD1	RXD1+	1	E-4	C-1	1
PortA2	RXD1	RXD1-	2	D-4	A-1	31
PortA3	TXD1	TXD1+	3	C-4	C-2	61
PortA4	RXCLK1	TXD1-	4	B-4	A-2	91
PortA5	No Connect	CLKIN+	5	A-4	C-3	2
PortA6	TXCLK1	CLKIN1-	6	E-5	A-3	32
PortA7	RTS1	CLKOUT1+	7	D-5	C-4	62
PortA8	CTS1	CLKOUT1-	8	C-5	A-4	92
GND	GND					3
GND	GND					33
PortB1	CD2	RXD2+	9	B-5	C-5	63
PortB2	RXD2	RXD2-	10	A-5	A-5	93
PortB3	TXD2	TXD2+	11	E-6	C-6	4
PortB4	RXCLK2	TXD2-	12	D-6	A-6	34
PortB5	No Connect	CLKIN2+	13	C-6	C-7	64
PortB6	TXCLK2	CLKIN2-	14	B-6	A-7	94
PortB7	RTS2	CLKOUT2+	15	A-6	C-8	5
PortB8	CTS2	CLKOUT2-	16	E-7	A-8	35
GND	GND					65
GND	GND					95
PortC1	CD3	RXD3+	17	D-7	C-9	6
PortC2	RXD3	RXD3-	18	C-7	A-9	36
PortC3	TXD3	TXD3+	19	B-7	C-10	66
PortC4	RXCLK3	TXD3-	20	A-7	A-10	96
PortC5	No Connect	CLKIN3+	21	E-8	C-11	7
PortC6	TXCLK3	CLKIN3-	22	D-8	A-11	37
PortC7	RTS3	CLKOUT3+	23	C-8	C-12	67
PortC8	CTS3	CLKOUT3-	24	B-8	A-12	97
GND	GND					8
GND	GND					38
PortD1	CD4	RXD4+	25	A-8	C-13	68
PortD2	RXD4	RXD4-	26	E-12	A-13	98
PortD3	TXD4	TXD4+	27	D-12	C-14	9
PortD4	RXCLK4	TXD4-	28	C-12	A-14	39
PortD5	No Connect	CLKIN4+	29	B-12	C-15	69
PortD6	TXCLK4	CLKIN4-	30	A-12	A-15	99
PortD7	RTS4	CLKOUT4+	31	E-13	C-16	10
PortD8	CTS4	CLKOUT4-	32	D-13	A-16	40
GND	GND					70
GND	GND					100
PortI1	No Connect	RXD9+	33	C-13	C-17	11
PortI2	RXD9	RXD9-	34	B-13	A-17	41
PortI3	TXD9	TXD9+	35	A-13	C-18	71
PortI4	No Connect	TXD9-	36	E-14	A-18	101
PortJ1	No Connect	RXD10+	37	D-14	C-19	12
PortJ2	RXD10	RXD10-	38	C-14	A-19	42
PortJ3	TXD10	TXD10+	39	B-14	C-20	72
PortJ4	No Connect	TXD10-	40	A-14	A-20	102
GND	GND					13
GND	GND					43

Table VIII : Pn4 and Molex Connector - Serial Interface Pin-outs

Notes :

1. PMC Pn4 pins route through to the host carrier cards (HCC) P0 or P2 depending on which Site the PMC is situated on.

2. P0 and P2 pin-outs have been checked on DY4's DVME-178 and DVME-190. Pin-outs on HCC may change.

3. Signals on Frontpanel Connector use a Molex Connector - P/N No. : 52755-1200 (120-pin, 1 mm Pitch Shielded Right Angle Connector) [Refer to Paragraph 6].

4. All other pins on the 120-pin Molex Connector are not connected to the adapter

5. Rear I/O pin-outs for CCII/SIO/PMC/4P/BP & CCII/SIO/PMC/4P/FP.

6. Front I/O pin-outs for CCII/SIO/PMC/4P/FP only.

7. CCII/SIO/PMC/4P/BP1 pin-outs are customer specific and not shown here.

4.3 LED Pin-outs (FP Adapter Only)

Reference	Status LED	Function	Comment	Color	Molex Pin No.
	LED3+	ALIVE	Connect To LED3 anode	Green	28
D3RET	LED3-	ALIVE_RET	Connect To LED3 cathode	-	58
D4	LED4+	USER	Connect To LED4 anode	D3	88
D4RET	LED4-	USER_RET	Connect To LED4 cathode	-	118

Table IX : LED Pin-outs

Notes :

1. The Status LEDs are current limited on the PMC Adapter.

2. Status LEDs '+' sign in 'LED[2..4]+' indicates the 'Anode' of the LED and the '-' sign indicates the 'cathode' of the LED.

4.4 BDM Connector

Pin No.	Signal Name	Signal Name	Pin No.
1	FVLS0	/SRESET	2
3	Ground	DSCK	4
5	Ground	VFSL1	6
7	/HRESET	DSDI	8
9	Vpp	DSDO	10

Table X : JH4 - BDM Connector

5. Programming Interface

5.1 Address Map

Address Range (Hex)	Mapping
0000 0000 – 000F FFFF	256 k x 32 Static RAM
7000 0000 – 7FFF FFFF	256 MBytes PCI memory for host access
F100 0000 – F100 0FFF	4 k QSpan registers.
FF00 0000 – FF00 FFFF	64 k PowerQUICC registers.
FFE0 0000 – FFFF FFFF	256 k x 32 Flash

5.2 PCI Configuration

The PCI configuration for the HSS PMC I/O Adapter is stored in the first 12 Bytes of the PCI configuration EEPROM. The contents of the EEPROM can be programmed via the QSpan's EEPROM Control and Status Register (EEPROM_CS) [2.2.1, page A-49]. The EEPROM_CS sits at offset 0x804 from the QSpan base register.

5.3 Non-volatile Memory

The HSS PMC I/O Adapter provides 2 MBytes of flash for boot-loader and application programming. The flash must be programmed via the BDM to ensure the proper set-up of the PowerQUICC memory controller. Once the flash has been programmed with a bootable image (i.e. an image that sets up the memory controller correctly) it may be re-programmed via the PCI interface or the BDM.

The PowerQUICC reset vector sits at either 0x100 or 0xFFF00100, depending on the reset state of D1 during reset. The choice of reset vector is made by placing R61 or not as follows:

R61 fitted - reset vector at 0xFFF00100

R61 not fitted - reset vector at 0x100

The first executable instructions in the bootable image should reside at the reset vector.

5.4 Interrupt Structure

The HSS PMC I/O Adapter uses interrupt INTA# on the PCI bus. To interrupt the adapter, four software programmable interrupts are available via the QSpan Interrupt Control Registers (INT_CTL & INT_CTL2). Refer to [2.2.1, Page A-41 and A-45] for more information on programming the interrupt registers.

The QSpan interrupts the PowerQUICC on /IRQ1. Refer to [2.2.2] for more information on processing PowerQUICC interrupts.

5.5 Base Address

The host PCI manager allocates the base address for the HSS PMC I/O Adapter. This allows the HSS PMC I/O Adapter to be mapped anywhere in PCI memory. The user must do a PCI find based on the Device ID, either (QSpan1 = 0x0860) or (QSpan2 = 0x0862), and the Vendor ID (0x10E3) to obtain a handle to the device. The base address of the adapter (the address of the QSpan) may then be read from PCI configuration space at offset 0x10.

5.6 Registers

For a full description of QSpan registers, refer to [2.2.1].

For a full description of PowerQUICC registers, refer to [2.2.2].

Note: PowerQUICC registers can not be accessed directly via the PCI bus.

6. **Molex Connector Pin-outs and Ordering Information**

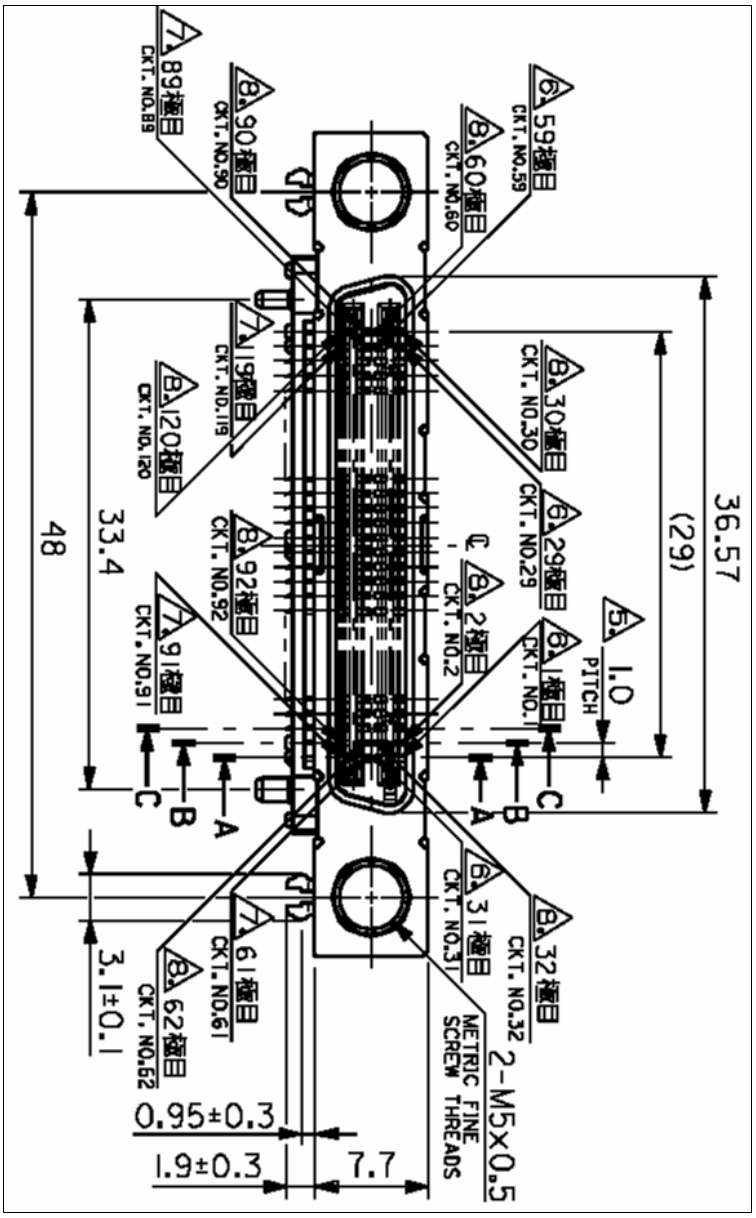

Figure 4 : Molex Connector Pin-outs

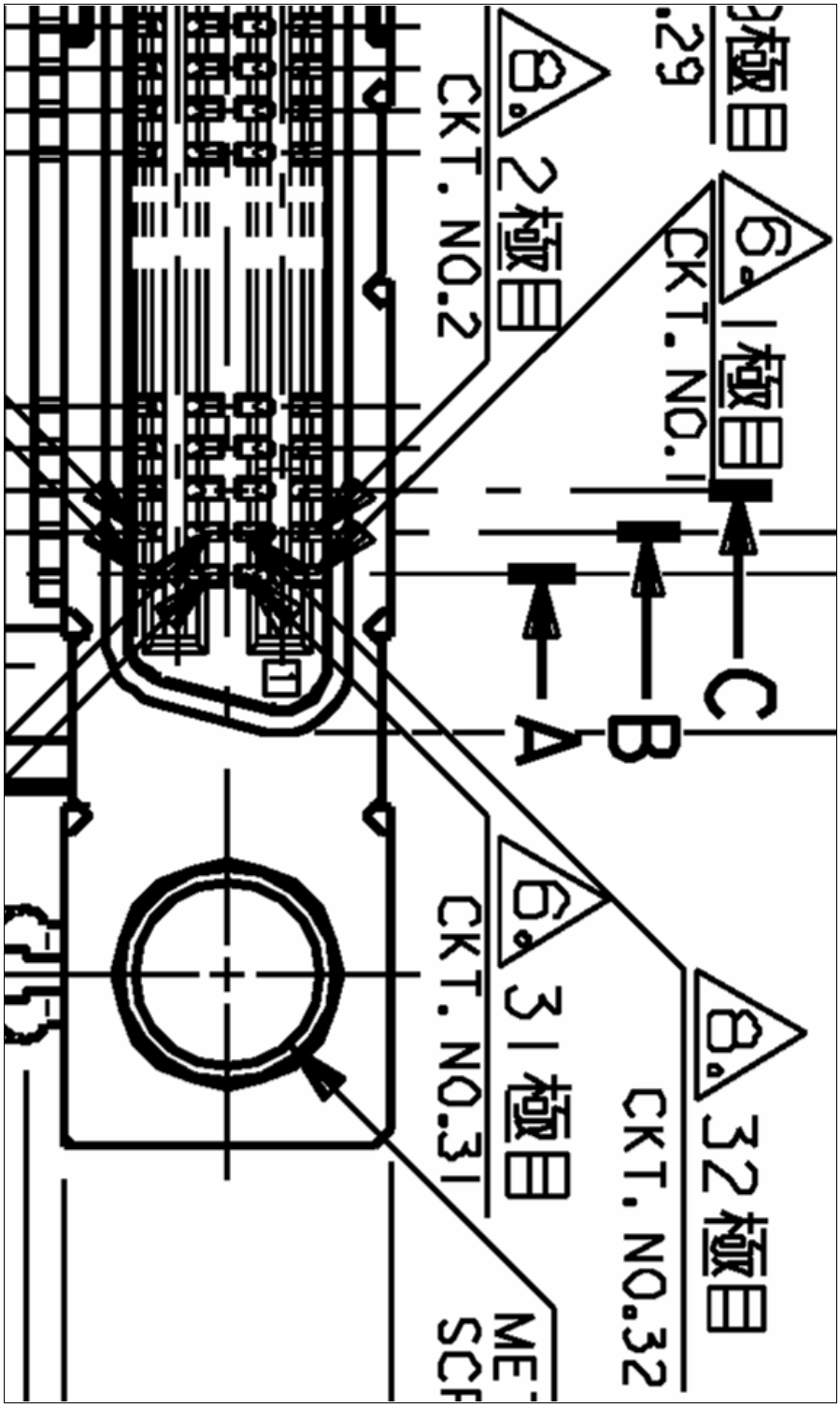

Figure 5 : Molex Connector Pin-outs (Large View of Part of Figure 4)

The Frontpanel connector on the PMC adapter, is a shielded right angle connector manufactured by MOLEX. A mating connector is supplied with the PMC adapter. However, should the need arise to obtain further mating connectors, the ordering information is given below :

Plug Assembly (Mating Connector)
Molex Part No. : 55032-1200

Cover Assembly (Mating Connector)
Molex Part No. : 58423-1200

Threaded Screw (Mating Connector)
Molex Part No. : 59811-0000

Above parts obtainable from the following agents :

Arrow Altech Distribution : (+27) (0)21-555 1884
Email : info@arrow.altech.co.za
URL : www.arrow.altech.co.za

Avnet Kopp : (+27) (0)21 689 4141
Email : sales@avnet.co.za
URL : www.avnet.co.za

The ordering information for the required ribbon cable is as follows :

1 mm Pitch Ribbon Cable 50 Way
Part Number : CABFAWG2850M

Above parts obtainable from the following agent :

Component Sources : (+27) (0)11 314 6844
Email : info@componentsources.co.za
URL : www.componentsources.co.za